PATENT SPECIFICATION

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COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Multilayer Printed Circuits

We, MULLARD LIMITED, a British Company, of Abacus House, 33, Gutter Lane, London, E.C.2. do hereby declare the invention, for which we pray that a patent may be granted to us, and the mtehod by which it is to be performed, to be particularly described in and by the following statement:

This invention relates to multilayer printed circuit assemblies.

Multilayer printed circuits of the kind comprising a plurality of individual circuit boards sandwiched together and bonded to form a single stacked assembly having interconnection between layers are well known. This kind of assembly makes for compactness where complex circuitry can be packed in a relatively small volume as well as affording good protection to the internal circuitry from adverse physical and environmental conditions. The sandwiching of the printed circuit layers can include the introduction of sealing compounds between layers thus making the inner layers impervious. Furthermore, the bonding of several layers increases the rigidity of the boards, which in themselves may be relatively thin, and this reduces any tendency to warping.

In order to provide electrical interconnection between and/or connections to circuit layers it is known to manufacture multilayer printed circuit assemblies in the following manner:

(a) A printed circuit design is processed in the normal manner on each internal board to be included in the stack. The stack may be arranged to present a conductive laminate in its external surfaces which are left unprocessed at this stage:

(b) Connection between or to any required internal layer is provided by predetermined positioning of a conductive laminate about a position for subsequent boring of a hole. Holes are bored through the stack in all interconnecting positions and the entire external surface, including the wall surfaces of interconnecting holes, are chemically plated with copper to form a plating electrode for the next step:

(c) The entire external surface of the assembly is now electroplated with copper. This reinforces the chemical plating of the interconnecting hole wall surfaces.

(d) A reversed resist image of the desired circuitry on each external plain surface of the stack is printed by silk screen method and a gold plating is deposited on all exposed surfaces including interconnecting hole surfaces. This provides a resist for the next step:

(e) The silk screen resist is now removed and the exposed copper laminate etched away leaving the gold plated laminate circuit design as the final circuit pattern together with through conduction for selected interconnecting hole surfaces.

The known method of manufacturing multilayer printed circuit assemblies as described above suffers from certain disadvantages. The ultimate definition of the final circuit design is limited by the use of the silk screen process. Furthermore, apart from the extra cost of gold plating, it has been found that gold plating can give rise to eventual embrittlement of subsequent soldered joints.

According to this invention there is provided a method of manufacturing a multilayer printed circuit assembly of the kind herein referred to, which includes the steps of chemically plating the external surfaces and interconnecting hole surfaces, thereafter electro-plating the entire assembly including said hole surfaces, sealing each of said holes with a removable filler or plug to

prevent the ingress of subsequent processing liquids, coating the entire outer surface with a photo-resist and processing the outer surfaces to the required circuitry and removing said fillers or plugs.

In this novel method of manufacturing multilayer printed circuit assemblies no gold plating is necessary and photographic accuracy of definition is obtained on external printed circuitry.

When a filler is used to seal off the interconnecting holes it may comprise an inert substance which is non-reactive in the presence of processing liquids. It has been found, for example, that an aqueous paste comprising a mixture of talc and sucrose in the proportions 4:1 will provide good sealing properties to subsequent processing liquids and at the same time can be easily removed after processing by use of warm water and an air jet.

When plugs are used to seal the holes prior to final processing the plugs may be pre-formed of a synthetic material which will afford full protection to the inner conductive hole surface but which can be simply removed after final processing by application of a plug solvent or body ejected by hydraulic, pneumatic or mechanical means.

In order that the invention may be clearly understood a method of manufacturing a multilayer printed circuit assembly according to this invention will now be described with reference to the accompanying drawings in which:

Figure 1 is an exploded view of a stack of four printed circuit boards in which the inner boards have been processed to the required circuit pattern.

Figure 2 shows an end section through A-A of Figure 1 and

Figures 3 to 5 show an enlarged detail of Figure 2 during various processing stages.

In Figure 1 four laminated circuit boards 1 to 4 are positioned one above the other by suitable guide means (not shown); boards 2 and 3 are provided with predetermined printed circuit patterns 5-5A, 6-6A and 7-7A; board 3 is provided with printed circuits on both plain surfaces and thus allows boards 1 and 4 to present an unprocessed conductive laminate on both upper and lower surfaces 8 and 9. The printed circuits on boards 2 and 3 have been provided with a predetermined circuit pattern which will allow for eventual interconnection of selected layers within the stacked assembly. The portion of the circuit 5 on board 2 is seen to have a conductive surface which extends up to a point 10 which is positioned immediately above a similar point 11 on board 3. However, circuit 7 on the underside of board 3 has been processed to provide an insulating space 12 which eventually disconnects the circuit of the joint circuits 5 and 6 from circuit 7. Similarly, it can be seen that circuit 5A on board 2 will be insulated from the circuits 6A and 7A.

In the next step the individual boards are stacked and held in registration by dowel pins (not shown) to ensure correct alignment and are then bonded under pressure to form a whole. The adhesive may be any suitable type, for example boards using a glass fibre/epoxy resin base can be bonded with an adhesive sold under the trade mark ARALDITE type AY/105/HY/956 which has a sufficiently long pot life at room temperature to allow the boards to be stacked and put under pressure before is viscosity becomes too great. Prior to use the adhesive should be out-gassed in a vacuum. A liberal amount of adhesive is applied to each internal board surface and the boards are located in correct stacked registration with one another with the aid of a suitable jig. The assembly is then placed under pressure so that the adhesive is squashed out so as to remove any air trapped between the layers. After the adhesive is cured and set, holes are drilled through the layers from one external conductive surface to the other to coincide with the predetermined interconnecting points. The accuracy of the drilling operation is assisted by a suitable template held in registration with the assembly jig.

Reverting now to the drawings, Figure 2 illustrates a section taken through A-A of Figure 1 in which the boards 1 to 4 have been bonded together and holes 13 and 14 have been drilled to provide eventual interconnection between selected internal printed circuits. It will be seen that hole 13 now traverses the conductive layer 8 and also conductive portions 5, 6 and 9. The processed portion 12 of the printed circuit 7 of board 3 is electrically insulated from the walls of hole 13 and the space caused thereby has been filled by the adhesive. In the next step all external surfaces, including the internal surface of the holes, are made electrically conductive by chemical deposition of copper, thus providing an electrode for subsequent electro-deposition of relatively heavy copper plating over the entire surface of the assembly.

Figure 3 shows a detail of the interconnecting hole 13 of Figure 2 to an enlarged scale, after an electro-plated copper layer 15 has been deposited. The copper plate around hole 13 now provides conductivity between laminate 8 of board 1, printed circuit 5 of board 2, printed circuit 6 of board 3 and laminate 9 of board 4, no connection being provided for printed circuit 7 on board 3.

In the next step, shown in Figure 4, the hole 13 has been sealed with a filler material 16 which is in the form of a paste consisting of a mixture of talc and sucrose in the ratio of 4:1 and mixed into a smooth

paste with water. The filler is allowed to dry and is then rendered flush with the external surface 15. The whole assembly is then dip coated with a photo-resist and the circuit pattern for the external surfaces which is in registration with the internal layer circuits and interconnecting holes, is then exposed to the photo-resist in the normal manner and developed. Removal of the unexposed resist results in the usual formation of a resist pattern 17 conforming to the desired circuitry, it will be seen that the circuit pattern on the upper surface8 includes a resist pattern 17 which includes the conductive surface 15 of hole 13. The resist pattern on lower laminate 9 exposes a ring 18 about the lower hole conduction surface 15 for eventual isolation of the interconnecting hole from the circuit pattern on laminate 9.

In the final steps, the unprotected portions of the external circuitry are etched away and the hole filler 16 is removed with the aid of warm water and an air jet. The final result is shown in Figure 5, where the hole 13 now provides electrical conduction for printed circuit pattern 8 of board 1 to circuit 5 of board 2, circuit pattern 6 of board 3 but not circuit 7 of board 3 nor circuit 9 of board 8. In the design of the individual boards prior to assembly provision is made of a selvedge strip around the outer edges of each board which of course becomes plated and electrically conductive. These edge strips are trimmed off after the final processing with a routing tool having its cutting edge moving parallel with the layers to reduce risk of one circuit smearing into contact with an adjacent circuit layer.

In the above description the assembly has been shown having only four layers and the number of communicating holes reduced for the sake of clarity. In practice, an assembly, for example as used in computer circuitry, might comprise ten layers of circuit boards measuring 150 mm × 180 mm which may have a total stacked thickness of only 1.5 mm. Such a board may have anything up to 3,000 or 4,000 interconnecting holes processed in the manner hereinbefore described.

WHAT WE CLAIM IS:—

1. A method of manufacturing a multilayer printed circuit assembly of the kind hereinbefore referred to which includes the steps of chemically plating the external surfaces and interconnecting hole surfaces, thereafter electro-plating the entire assembly including said hole surfaces, sealing each of said holes with a removable filler or plug to prevent the ingress of subsequent processing liquids, coating the entire outer surface with a photo-resist and processing the outer surfaces to the required circuitry and removing said hole fillers or plugs.

2. A method of manufacturing a multilayer printed circuit assembly as claimed in Claim 1 wherein the said filler comprises an inert substance which is non-reactive in the presence of processing liquids.

3. A method of manufacturing a multilayer printed circuit assembly as claimed in Claim 2, wherein said filler comprises a mixture of talc and sucrose mixed with water in the form of a paste.

4. A method of manufacturing a multilayer printed circuit assembly as claimed in Claim 3, wherein said mixture comprises talc and sucrose in the proportion of 4:1.

5. A method of manufacturing a multilayer printed circuit board as claimed in Claim 1, wherein said hole plug comprises a pre-formed plug.

6. A method of manufacturing a multilayer printed circuit assembly as described herein with reference to the accompanying diagrammatic drawings.

7. A multilayer printed circuit assembly fabricated in accordance with any of the preceding claims.

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1,042,234 COMPLETE SPECIFICATION
1 SHEET

This drawing is a reproduction of the Original on a reduced scale.

FIG. 1.

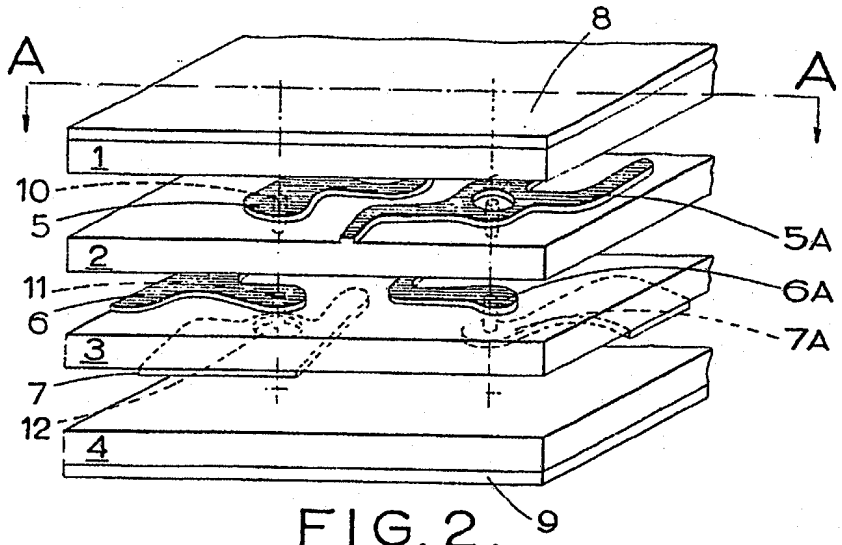

FIG. 2.

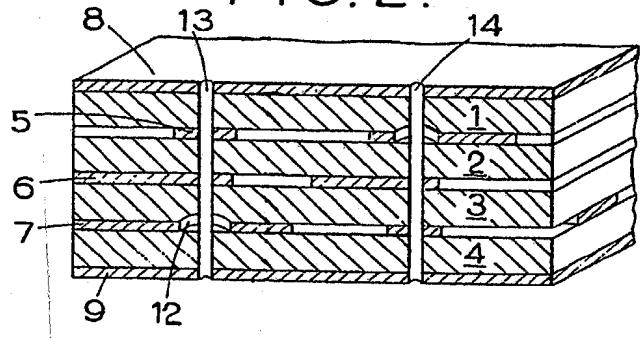

FIG. 3.

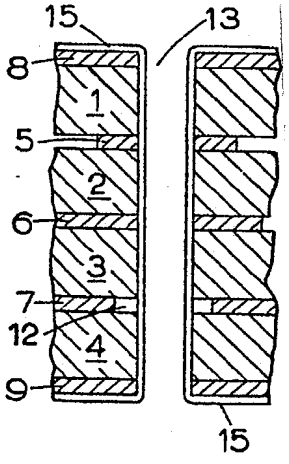

FIG. 4.

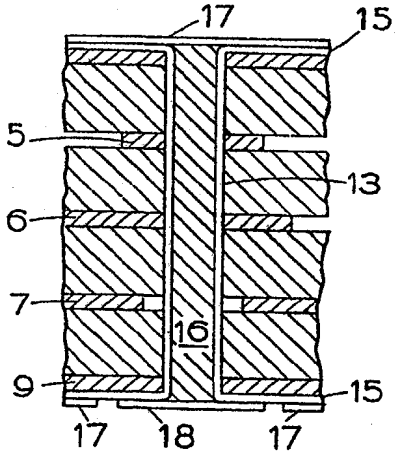

FIG. 5.